Novel Asymmetric Gate-Recess Engineering for Sub-Millimeter-Wave InP-based HEMTs

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***Abstract* — A self-aligned asymmetric gate-recess structure for ultra-high speed InGaAs/InAlAs high electron mobility transistors (HEMTs) is successfully fabricated. A 50-nm-T-shaped-gate HEMT with a longer drain-side recess exhibits a much-improved maximum oscillation frequency (f_{max}) of 503 GHz with keeping a similarly high current-gain cutoff frequency (f_t) of 307 GHz compared to that with a conventional symmetric recess structure. This result indicates reduced electric field between gate and drain with keeping a small source resistance (R_s) in the developed asymmetrically recessed HEMT.**

I. Introduction

InP-based InGaAs/InAlAs high electron mobility transistors (HEMTs) are considered to be one of the most promising devices for millimeter-wave and optical communications because of their superior high frequency and low noise performances. This is due to high electron mobility, high saturation velocity, and high sheet carrier density obtained in this system. A shorter gate is essential for the ultra-high RF performance. In fact, RF performances have been significantly improved by reducing gate length (L_g) down to 50 nm or below, which increased the current-gain cutoff frequency (f_t) above 350 GHz [1, 2]. Another important device property that characterize high frequency performance is the maximum oscillation frequency (f_{max}), which is given by

$$f_{max} = f_t / [4 \cdot g_d \cdot (R_s + R_i + R_g) + 2 \cdot (C_{gd} / C_{gs})((C_{gd} / C_{gs}) + g_m \cdot (R_s + R_i))]^{1/2} \quad (1)$$

where R_s, R_i, R_g, g_d, g_m, C_{gs} and C_{gd} represent equivalent network elements. An optimization of f_{max} can be achieved by minimizing these elements except for g_m with keeping a high f_t. A higher In content (>0.7) of a pseudomorphic InGaAs channel layer increases f_t, however, it also increases drain-conductance g_d because of enhanced impact ionization due to smaller band-gap (E_g) of InGaAs, and then limits f_{max} [3]. Gate-recess length (L_r), the length of the recessed region adjacent to the gate electrode, is another important parameter to control these elements. A shorter source-side recess gives a smaller source-resistance (R_s), therefore, a higher g_m and f_t. On the other hand, a longer drain-side recess relaxes the electric field between gate and drain, which may suppress the impact ionization and then result in a smaller g_d. Hence, the asymmetric gate-recess structure is effective in that it enables independent optimization of each side recess length to achieve a higher device performance.

In this paper, we have developed a self-aligned asymmetric gate-recess fabrication technique for ultra-short T-shaped-gate HEMTs, and achieved a much-improved f_{max} of 503 GHz with keeping a high f_t of 307 GHz in a 50-nm pseudomorphic HEMT with an asymmetric recess structure.

II. Source Resistance Extraction

The HEMT epitaxial structure used in this work consists of an InAlAs buffer layer (300 nm), a pseudomorphic InGaAs (In content x = 0.7) channel layer (12 nm), an InAlAs spacer layer (3 nm), Si planar doping (5×10^{12} cm^{-2}), an InAlAs barrier layer (10 nm), an InP etch-stopper layer (6 nm), and a Si-doped InGaAs cap layer (20 nm), which was grown on a semi-insulating (100) InP substrate by metal organic chemical vapor deposition (MOCVD). The electron mobility of the two-dimensional electron gas is 10500 cm^2/V$\cdot$ s and the sheet carrier density is 1.9×10^{12} cm^{-2} at room temperature, which was measured after the n$^+$-InGaAs cap layer was removed down to the InP etch-stopper layer by wet chemical etching.

In order to investigate recess length (L_r) dependence of the source resistance (R_s), we proposed a simple method to

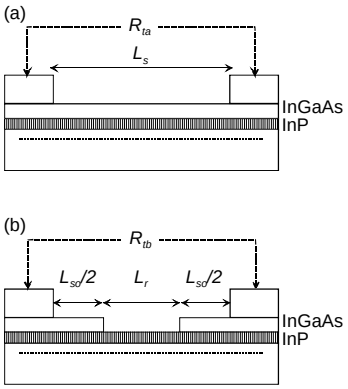

Fig. 1. TLM test patterns for an extraction of contact resistance (R_c) and sheet resistances (R_{capped}, $R_{recessed}$) of capped (*a*) and recessed (b) regions.

extract sheet resistances of capped (R_{capped}) and recessed ($R_{recessed}$) regions, which is based on a well-known transmission line model (TLM). Figure 1 shows schematic illustrations of two TLM test patterns used in this experiment. Fig. 1a shows a conventional TLM pattern to extract the contact resistance (R_c) and R_{capped}, in which spacing (L_s) between two ohmic contact pads was changed from 2.5 to 40 µm. Fig. 1b shows another TLM pattern to extract $R_{recessed}$, in which the recess length (L_r) was changed from 0.6 to 8.1 µm while keeping the length of remaining capped region to be constant (L_{so} = 2.0 µm). Total resistances (R_{ta}, R_{tb}) between two contact pads for two TLM samples linearly changed with respect to L_s and L_r. As a result, R_c, R_{capped} and $R_{recessed}$ were found to be 0.10 ohm· mm, 108 ohm/sq. and 243 ohm/sq. respectively using following equations:

$$R_{ta} = 2\cdot\ R_c + L_s\cdot\ R_{capped}/W \qquad (2)$$

$$R_{tb} = 2\cdot\ R_c + L_{so}\cdot\ R_{capped}/W + L_r\cdot\ R_{recessed}/W \qquad (3)$$

where W represents the width of the transmission line. Using these values, R_s, which is defined as (R_c + R_{capped} + $R_{recessed}$), was estimated as a function of a source-side recess length (L_{rs}) for an actual HEMT device with a source-drain separation (L_{sd}) of 2 µm and a gate width (W_g) of 100 µm as shown in Fig. 2. Since the $R_{recessed}$ value is 2.3 times larger than R_{capped}, R_s linearly increases with increasing L_r by 1.35 × 10^{-3} ohm/nm. Supposing an intrinsic transconductance (g_{mi}) of a device is 1.0 S/mm, an extrinsic transconductance (g_m) is estimated as a function of L_{rs} as shown in Fig. 2 according to a following equation:

$$g_m = g_{mi} / (1 + R_s\cdot\ g_{mi}). \qquad (4)$$

From the view point of g_m, the source-side recess length should be as small as possible.

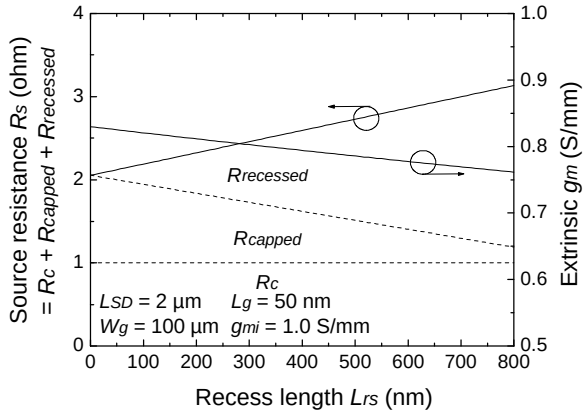

Fig. 2. Estimated source resistance (R_s = R_c + R_{capped} + $R_{recessed}$) and extrinsic transconductance (g_m) as a function of recess length (L_{rs}) for an actual device with L_{sd} = 2 µm, W_g = 100 µm and g_{mi} = 1.0 S/mm.

III. Asymmetric Gate Recess Fabrication

In our previous paper, we have demonstrated a sub-50-nm T-shaped-gate fabrication technique using a conventional tri-layer resist system [4]. Recently, we could realize an excellent intrinsic f_t as high as 387 GHz in a 30-nm pseudomorphic HEMT, which is the highest value ever reported for any transistors as shown in figure 3.

In order to further improve the device performance, especially for f_{max}, we have developed an asymmetric gate-recess fabrication technique for ultra-short T-shaped-gate HEMTs. Figure 4 summarizes the fabrication process flow. A tri-layer resist consisting of a bottom 180-nm-thick ZEP layer, a middle 450-nm-thick PMGI layer and a top 240-nm-thick ZEP layer, is coated on a SiO_2 film thermally evaporated on the wafer to improve resist adhesion (Fig. 4a). The top and middle layers are exposed simultaneously with a relatively low dose so as not to affect the bottom layer, and developed using a high sensitive developer. The bottom layer is then exposed with a high dose, and developed using a low sensitive developer. The bottom pattern consists of a main gate pattern with a pattern size of L_g and additional small slit patterns separated from the main pattern by l toward the drain-side, whose size is $a \times b$ and spacing c. (Fig. 4b). Next, the SiO_2 film is etched through these patterns by reactive ion etching (RIE) using CF_4, which enables precise replication of sub-50 nm patterns [4]. Wet chemical etching using an aqueous solution of $C_6H_8O_7$ and H_2O_2 mixture forms a gate-recess structure in the n^+-InGaAs cap layer (Fig. 4c). It should be noted that recess etching occurs through the small slit patterns as well as the main gate pattern. The source- and drain-side recess lengths (L_{rs}, L_{rd}) can be independently

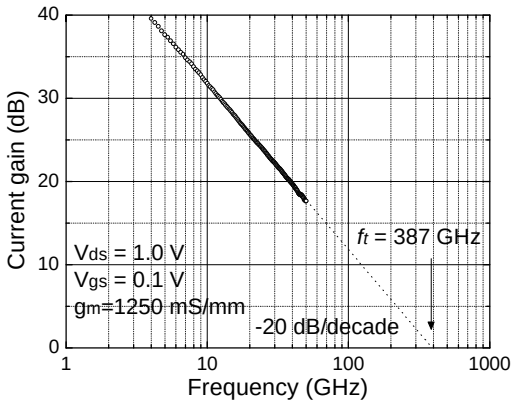

Fig. 3. Frequency dependence of current gain ($|h_{21}|^2$) of recently developed 30-nm pseudomorphic HEMT.

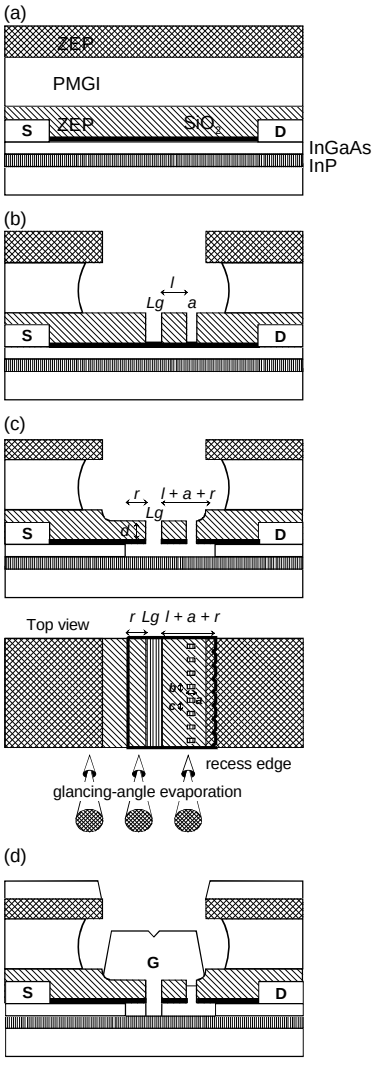

Fig. 4. Fabrication process flow of T-shaped gate with an asymmetric gate-recess structure.

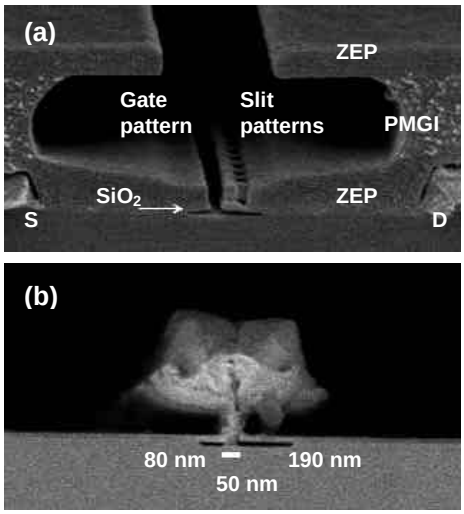

Fig. 5. Bird's-eye and cross-sectional SEM photographs of a recessed sample before evaporation (a) and T-shaped-gate after lift-off (b) when L_g = 50 nm, r = 80 nm, l = 60 nm, a = 50 nm, b = 20 nm and c = 80 nm.

controlled by a recess etching length (r) and ($l + a + r$) respectively. Finally, a gate metal is evaporated from a direction with a glancing-angle q, where $q > \tan^{-1}(b/d)$ (d: bottom resist thickness after RIE), not to be evaporated on the semiconductor surface under the slit patterns (Fig. 4d). Figure 5 shows bird's-eye and cross-sectional SEM photographs of a recessed sample before evaporation (Fig. 5a) and T-shaped-gate after lift-off (Fig. 5b) when L_g = 50 nm, r = 80 nm, l = 60 nm, a = 50 nm, b = 20 nm and c = 80 nm. A 50-nm-T-shaped-gate with a well-controlled asymmetric recess structure with L_{rs} of 80 nm and L_{rd} of 190 nm was thus successfully fabricated.

IV. Device Characterization

Figure 6 shows the frequency dependence of the current gain $|h_{21}|^2$ and Mason's unilateral power gain U_g of fabricated 50-nm pseudomorphic HEMT with the symmetric (Fig. 6a) and asymmetric recess structure (Fig. 6b) when biased at drain-source voltage (V_{ds}) of 1.2 V and gate-source voltage (V_{gs}) of –0.4 V. Almost the same f_t of 307 GHz was achieved in the asymmetric sample as that (322 GHz) for the symmetric sample. On the other hand, f_{max} of the asymmetric sample was increased up to 503 GHz, which is 80% larger than that (281 GHz) for the symmetric sample. Figure 7 shows extracted g_m and g_d from measured S-parameters for these samples as a function of V_{ds} when V_{gs} = –0.4 V. As for g_m, both samples showed almost the same value, which is considered to result from the same source-resistance R_s due to the same

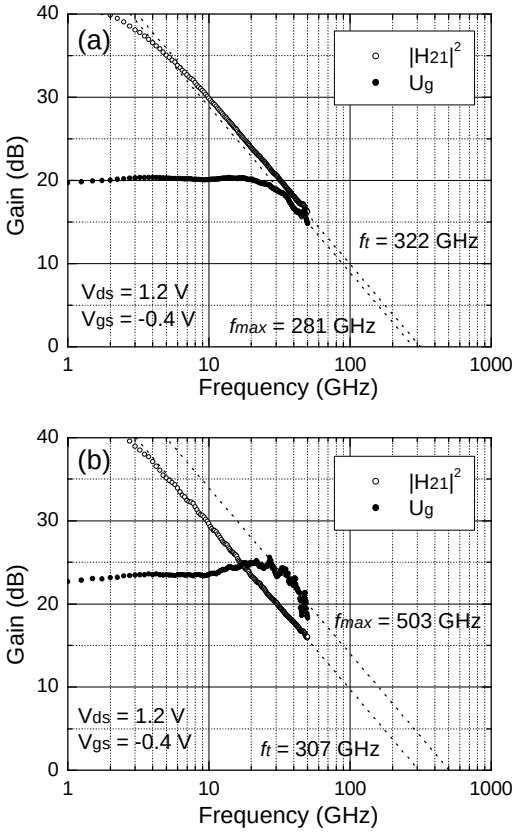

Fig. 6. Frequency dependence of current gain $|h_{21}|^2$ and Mason's unilateral power gain U_g of 50-nm-gate HEMT with symmetric (a) and asymmetric recess structure (b) biased at V_{ds} = 1.2 V and V_{gs} = -0.4 V.

L_{rs}. It is noteworthy that g_d value of the asymmetric sample was reduced by 27% compared to the symmetric one, which can be attributed to the reduced electric field between gate and drain due to a longer L_{rd}, and therefore, reduced impact ionization. Thus, the asymmetric recess structure is very effective to reduce g_d with keeping a small R_s, and result in a higher f_{max}. Furthermore, on-state breakdown voltage (BV_{on}) was also improved from 2.1 V to 2.4 V due to the reduced electric field by utilizing the longer L_{rd}.

V. Conclusion

We proposed a new self-aligned asymmetric gate-recess fabrication method for ultra-short T-shaped-gate HEMTs, and demonstrated a 50-nm pseudomorphic HEMT with an asymmetric recess structure, which exhibited a much-improved f_{max} by reducing g_d and R_s. This technique is considered to become more effective when L_g becomes

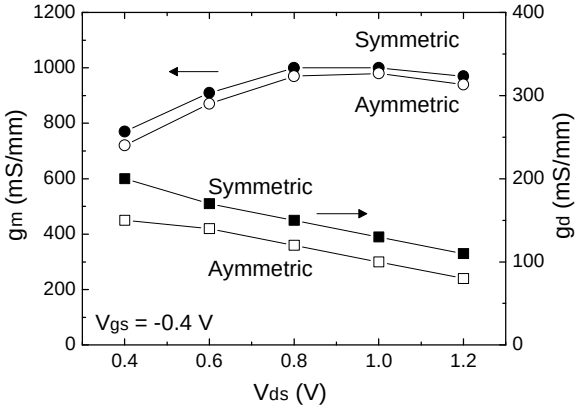

Fig. 7. g_m and g_d extracted from measured S-parameters for symmetric (solid) and asymmetric (open) samples as a function of V_{ds} at V_{gs} = –0.4 V.

smaller, since the reduced gate-to-channel distance, i.e., the thinner barrier layer, to suppress "short-channel effect"may cause an increase in the resistance of the recessed region ($R_{recessed}$) and then R_s.

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